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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,615	10/06/2003	Grant H. Kobayashi	42P17527	5561

59796 7590 03/20/2007

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EXAMINER	
KNOLL, CLIFFORD H	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/680,615	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *20-42 and 53-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 43-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/6/03,3/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19 and 43-52, drawn to class 710/267.

II. Claims 20-42 and 53-58, drawn to class 711/147.

Inventions I and II are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different designs, modes of operation, and effects (MPEP § 802.01 and § 806.06). In the instant case, the invention of groups I and II are found in different classes, one relating to interrupt processing, and the other to shared memory.

During a telephone conversation with Dave McAbee (#58104) on 3/6/06 a provisional election was made without traverse to prosecute the invention of group I, claims 1-19 and 43-52. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-42 and 53-58 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

2. Claims 9 and 49-50 are objected to because of the following informalities:

In claim 9, "the register" lacks antecedent basis. If "a register" is intended, it should be so recited.

In claims 49 and 50, "the storage device" lacks antecedent basis. If "a storage device" is intended, it should be so recited.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. *Claims 1-11, 13-15, 17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Gephardt (US 5781187 A).*

Regarding claim 1, Gephardt discloses waiting if the second is active (e.g., col. 21, lines 37-39), and handling the SMI on both processors if the second processor is active and in the SMI mode (e.g., col. 21, lines 61-65), and handling the SMI with the

first processor if the second processor is inactive (e.g., col. 21, lines 35-39, in the event the SMI does not affect other processors they are deemed to be inactive with respect to the current SMI).

Regarding claim 2, Gephardt also discloses examining a storage medium by the first processor to determine the second processor's state (e.g., col. 21, lines 63-65).

Regarding claim 3, Gephardt also discloses system memory (e.g., col. 21, lines 63).

Regarding claim 4, Gephardt also discloses the synchbyte (e.g., col. 21, lines 44-47).

Regarding claim 5, Gephardt also discloses the synchbyte has a value representing an inactive state (e.g., col. 21, line 58, "RETURN" considered "an inactive state").

Regarding claim 6, Gephardt also discloses a value representing the second processor in an active but not SMI mode (e.g., col. 21, line 43, "HOLD" considered an active but not SMI mode).

Regarding claim 7, Gephardt also discloses a value representing an active and SMI mode (e.g., col. 21, line 59, "SHUTDOWN").

Regarding claim 8, Gephardt also discloses the system register (e.g., col. 21, line 45).

Regarding claim 9, Gephardt also discloses a register is located in the second processor (e.g., col. 21, line 43).

Regarding claim 10, Gephardt also discloses the default state is an inactive state (e.g., col. 22, lines 10-14).

Regarding claim 11, Gephardt also discloses updating the storage medium with the second processor (e.g., col. 16, lines 50-55).

Regarding claim 13, Gephardt also discloses writing a value representing if the second processor is waking-up and not in SMI state (e.g., col. 21, line 43).

Regarding claim 14, Gephardt also discloses writing a value representing if the second processor is entering SMI mode (e.g., col. 21, lines 58-59).

Regarding claim 15, Gephardt also discloses generating an SMI before receiving it (e.g., col. 4, lines 11-13).

Regarding claim 17, Gephardt also discloses generating the SMI through hardware (e.g., col. 21, lines 66-67).

Regarding claim 19, Gephardt also discloses physical processors (e.g., col. 1, lines 31-34).

4. Claims 43, 45-46, and 51-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Cooper (US 7152169 B2)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 43, Cooper discloses the controller hub (e.g., col. 3, lines 22-23), and storage medium coupled to the first and second processor (e.g., col. 5, lines 63-65) where the first processor checks the system management state of the second processor (e.g., col. 4, lines 62-64).

Regarding claim 45, Cooper also discloses waiting for the second processor to enter the SMI state if active and not in the SMI mode (e.g., col. 4, lines 60-62).

Regarding claim 46, Cooper also discloses handling the SMI on both processors if the second process state is active and in SMI mode (e.g., col. 4, lines 65-67).

Regarding claim 51, Cooper also discloses logical processors (e.g., col. 3, lines 11-12).

Regarding claim 52, Cooper also discloses physical processors (e.g., col. 3, lines 56-59).

5. Claims 43, 47-49, and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen.

Regarding claim 43, Nguyen discloses the controller hub (e.g., Fig. 1, "16") and system management state checked by the first processor after an SMI (e.g., para. 18).

Regarding claim 47, Nguyen also discloses system memory (e.g., para. 18, SMRAM).

Regarding claim 48, Nguyen also discloses a synchbyte (e.g., para. 18, "software SMI signature").

Regarding claim 49, Nguyen also discloses a register (e.g., para. 18, SMRAM).

Regarding claim 52, Nguyen also discloses physical processors (e.g., para. 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. *Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt as applied supra, in view of Jain (US 20040225907 A1).*

Regarding claim 12, Gephardt does not expressly mention writing a value representing if the second processor is going into inactive state; however Jain discloses this (e.g., Fig. 3, "300"). It would have been obvious to one of ordinary skill in the art to combine Jain with Gephardt, because Jain provides a means to transition to low power mode in a system such as Gephardt, thus conserving power.

7. *Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt as applied supra, in view of Nguyen (US 20020099893 A1).*

Regarding claim 16, Gephardt does not expressly mention generating a software SMI; however this is commonplace as seen in Nguyen (e.g., para. 17). It would have been obvious to one of ordinary skill in the art to combine Nguyen because Nguyen

teaches a more flexible means of generating an SMI in a multiprocessor system such as that of Gephardt.

8. *Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt as applied supra, in view of commonplace implementation techniques, as evidenced by Olarig (US 6662272 B2).*

Regarding claim 18, Gephardt does not expressly mention logical processors; however, Examiner takes Official Notice that this is a widely known implementation technique for processors, as evidenced by Olarig (e.g., col. 1, lines 50-52). It would have been obvious to combine Gephardt with common implementations, because implementations of logical processors increases the flexibility of the hardware.

9. *Claims 43-49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt in view of Nishanov (US 20030065782 A1).*

Regarding claim 43, Gephardt discloses the controller hub (e.g., Fig. 2, "220"), a storage medium for storing a system management state of at least the second processor (e.g., Fig. 13), and checking the second processor after receiving an SMI (e.g., col. 21, lines 35-38). Gephardt also discloses determining if a processor is active (e.g., col. 21, lines 33-35), but does not expressly mention this determining uses a storage medium; however Nishanov discloses this (e.g., para. 40). It would have been obvious to one of ordinary skill in the art to combine Nishanov with Gephardt because

Nishanov teaches a particular implementation that will permit peripherals to be shared and identified by a multiprocessing system such as Gephardt.

Regarding claim 44, Gephardt also discloses handling the SMI with the first processor if the second processor is inactive (e.g., col. 21, lines 35-39, in the event the SMI does not affect other processors they are deemed to be inactive with respect to the current SMI).

Regarding claim 45, Gephardt also discloses waiting if the second is active (e.g., col. 21, lines 37-39).

Regarding claim 46, Gephardt also discloses handling the SMI on both processors if the second processor is active and in the SMI mode (e.g., col. 21, lines 61-65).

Regarding claim 47, Gephardt also discloses system memory (e.g., col. 21, lines 63).

Regarding claim 48, Gephardt also discloses the synchbyte (e.g., col. 21, lines 44-47).

Regarding claim 49, Gephardt also discloses the system register (e.g., col. 21, line 45).

Regarding claim 52, Gephardt also discloses physical processors (e.g., col. 1, lines 31-34).

10. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt and Nishanov as applied supra, in view of common memory types, as

evidenced by Goldman (US 6564371 B1).

Regarding claim 50, Gephardt does not expressly mention flash memory; however, Examiner takes Official Notice that it is a common memory type used in a system, as evidenced by Goldman (e.g., col. 5, lines 56-59). It would have been obvious to one of ordinary skill in the art to combine common memory types with Gephardt because use of flash allows for more robust storage of configuration information.

11. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gephardt and Nishanov as applied supra, in view of commonplace implementation techniques, as evidenced by Olarig.

Regarding claim 51, Gephardt does not expressly mention logical processors; however, Examiner takes Official Notice that this is a widely known implementation technique for processors, as evidenced by Olarig (e.g., col. 1, lines 50-52). It would have been obvious to combine Gephardt with common implementations, because implementations of logical processors increases the flexibility of the hardware.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3636. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Clifford H Knoll
Patent Examiner
Art Unit 2111

chk